3D on-chip data center networks using circuit switches and packet switches

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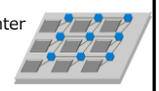
Research background

- Many data centers have been built
  - Online services treating a large amount of data become popular
    - Example: Search engines, online shopping
  - Such online services are provided by data centers
- The energy consumed by data centers becomes an important problem
  - We should construct the energy efficient data center

The energy efficient data center :
An on-chip data center[1]



- An on-chip data center is a chip performing a task of a data center with small energy consumption
- In an on-chip data center, many CPU cores are placed on a single chip, and network between the cores is constructed
  - CPU cores performs the tasks by cooperating with each other
  - This network plays an important role in this chip

[1] M. Kas, "Toward on-chip datacenters: a perspective on general trends and on-chip particulars," The Journal of Supercomputing, vol. 62, pp. 214-226, Oct. 2012.

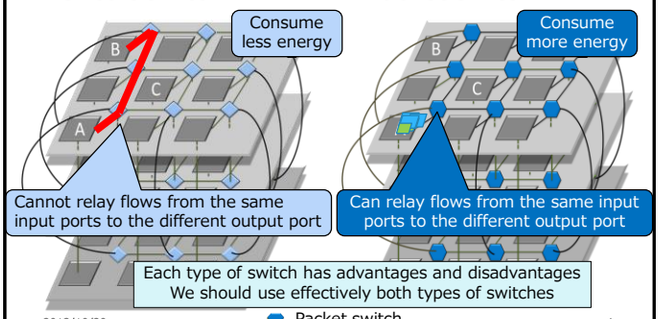
3D Network on Chip

- 3D Network on Chip(NoC) architecture
  - The 3D NoC[2] is constructed by stacking multiple 2D chip layers vertically
    - The vertically stacked layers decrease the number of hops between switches
    - The vertical links are significantly shorter than the horizontal links
      - The vertical links consume less energy than the horizontal links
- 3D NoC reduces both the energy consumption and the delay
  - We believe that the 3D NoC is the network architecture suitable to on chip data centers

[2] F. Li, C. Nicopoulos, T. Richardson, and Y. Xie, "Design and management of 3D multiprocessors using network-in-memory," in Proceedings of ISCA, pp. 130-141, June 2006.

Comparison between circuit and packet switches

- Circuit switch
- Packet switch



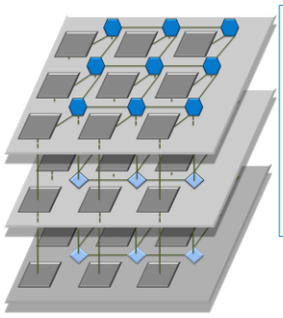
The goal of this research

Clarify the network structure suitable to the on-chip data center

- We considered to use both of circuit and packet switches as approach for minimizing energy consumption
  - Circuit switch
    - Consume less energy
    - Can not relay flows from different input ports to the same output port
  - Packet switch
    - Consume more energy
    - Can relay flows from different input ports to the same output port

The key point of this research is how to use these two types of switches

Our on-chip data center network

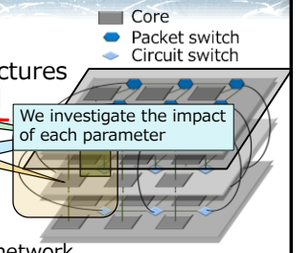


- Servers
  - Vertically stacked cores work as a single server
  - Each server is connected to one of packet switches
- Network
  - Network includes the packet and circuit switches
  - Switches are placed in 3D lattice
  - All switches without connection to servers are circuit switches

Core
Packet switch
Circuit switch

Evaluation

- Parameters of the 3D network structures
  - Connection from servers
  - Inter layer connection
  - Placement of switches within each layer
- Metrics
  - Energy consumed by the network
    - The sum of energy consumed by switches and links
  - Delay
    - The time required to receive all traffic by the destination cores after generating the traffic demands

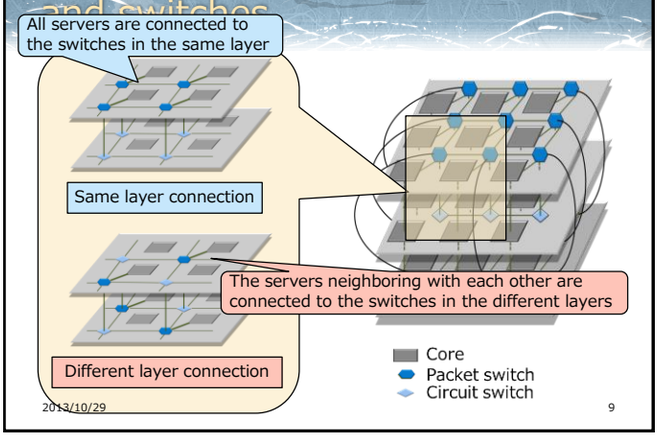


Environment

- Topology
  - The number of servers : 15*15
  - Length of intra layer link : 2mm
  - Length of inter layer link : 1um
- Traffic
  - Generated between randomly selected server pairs
    - The number of communicating server pairs: from 100 or 500
    - The amount of traffic between selected server pairs: 10,000 bit
- Routing
  - Set so as to minimize the energy consumed by the switches and links
- Energy consumption model
  - Model proposed in [3]

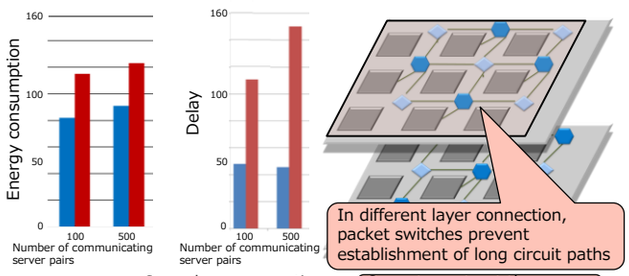
[3] P. T. Wolkotte, G. J. M. Smit, N. Kavaldjiev, J. E. Becker, and J. Becker, "Energy model of networks-on-chip and a bus," in *Proceedings of IEEE International Symposium on System-on-Chip*, pp.82-85, Nov. 2005.

Connection between servers and switches

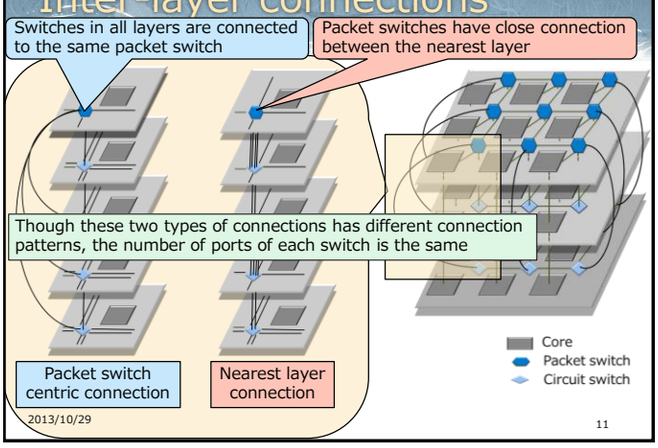


Comparison of the connection between servers and switches

- Same layer connection achieves both of less energy consumption and less delay

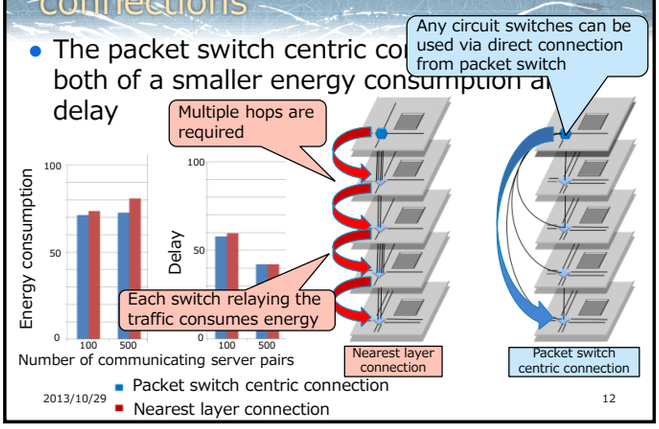


Inter-layer connections

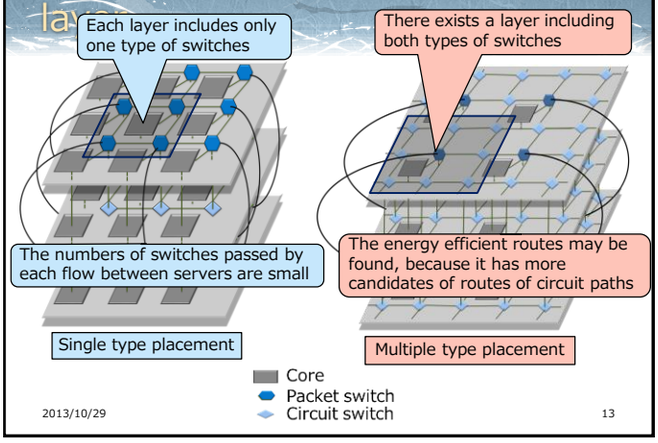


Comparison of Inter-layer connections

- The packet switch centric co… both of a smaller energy consumption a… delay



Placement of switches within a layer



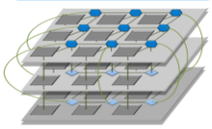
Comparison of the placement of switches within a layer

- Multiple type placement does not reduce the energy consumption and delay
  - We conclude that the single type placement is sufficient

Conclusion and future work

- Conclusion
  - We investigated the 3D on-chip data center network structures which use both of the circuit and packet switches
    - The servers should connect to the packet switches in the same layer
    - The packet switches should connect to the circuit switches in all layers
    - The layer including both of circuit and packet switches should be avoided

To achieve the smaller energy consumption and smaller delay



- Future work
  - The method to set the routes suitable to the on-chip networks

Model

- Energy consumption model[3]
  - Packet switch : 0.98μW/bit
  - Circuit switch : 0.37μW/bit
  - Link consumes : $(0.39+0.12L)$μW /bit
    (L : length of link (mm))
- Delay model
  - The time required to receive all traffic by the destination cores after generating the traffic demands
    - Each flit can be relayed by a packet switch to the next packet switch in 1 clock cycle
    - The relay of the flits by the circuit switch takes no clock cycles
      - The delay between cores depends only on the number of packet switches passed by the flow

[3] P. T. Wolkotte, G. J. M. Smit, N. Kavaldjiev, J. E. Becker, and J. Becker, "Energy model of networks-on-chip and a bus," in *Proceedings of IEEE International Symposium on System-on-Chip*, pp.82-85, Nov. 2005.